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A New Medium Voltage Modular Multilevel Inverter with Advanced Carrier-Based Pulse Width Modulation for Solar Photovoltaic Systems

Md. Tariqul Islam[1], Md. Rabiul Islam[2], Md. Shizer Rahman[3], Md. Fayzur Rahman[4], Md. Ashib Rahman[5]

[1,3]Department of Electrical and Electronic Engineering, Pundra University of Science & Technology, Bogura, Bangladesh

[2,5]Faculty of Engineering and Information Sciences, University of Wollongong, New South Wales 2522, Australia

[4]Department of Electrical and Electronic Engineering, Green University of Bangladesh

ashamim617@gmail.com[1]; mrislam@uow.edu.au[2]; rshizer@yahoo.com[3]; drfayzur@green.edu.bd.com[4]; mar997@uowmail.edu.au[5]

Abstract— For medium and high-power applications, reduced switch multilevel inverters (MLI) have drawn considerable attention from the industry and the academia alike due to their diverse benefits like the requirement of a smaller number of voltage sources and switching devices, and better control functionalities compared to the traditional MLI topologies. In this paper, a new symmetric MLI is proposed for the grid integrated photovoltaic (PV) power generation system. An extensive comparison demonstrates that the number of the switching devices with the proposed topology is less in comparison to that of the existing MLI topologies, which is the main objective of this paper. The proposed topology is simulated in MATLAB/Simulink to carry out the necessary analysis and comparisons to the existing ones in terms of the number of switching devices and power diodes, cost, weight, and the percentage of total harmonic distortion. Simulation results demonstrate that the proposed topology uses only 67% switching devices and 40% power diodes than other MLI topologies to generate 15 level output voltage with low total harmonic distortion than existing topologies. Due to the reduced switching devices and power diodes count, the proposed topology offers less switching loss as well as increased efficiency with the reduced overall system cost. The proposed MLI topology has a great potential for the industry applications and the realization of a sustainable solar PV system.

Keywords— multilevel inverter, grid integration, switching technique, total harmonic distortion, switching loss, system cost.

I. INTRODUCTION

The multilevel inverter (MLI) has been proved to be a potential candidate for the grid integration of renewable energy sources due to several benefits like low harmonic distortion, high efficiency and lower voltage stress on the switches [1]. The term 'multilevel' was primarily started with the three level and later it has been raised to N number of levels. Generally, the family of MLIs are categorized as diode clamped (DC) MLI, cascaded H-bridge (CHB) MLI, flying capacitors (FC) based MLI, Neutral point clamped (NPC) MLI [2]. Despite the fact that these classes of MLIs are broadly utilized in high power applications, they have some drawbacks. The principle downside of NPC topology is unequal dc connection and requirement for higher number of clamping diodes. FC topology uses flying capacitor as clamping device yet for higher voltage application needs an inordinate number of storage capacitors. Among these topologies, CHB is an appropriate choice for high voltage application because of its modularity and straightforwardness from the controller design viewpoints [3]. In CHB MLI, H bridge cells are connected in series for providing multilevel output. Each H-bridge cell consists of four switches and one voltage source. The number of voltage levels in this inverter can be increased by adding additional H-bridge cells. These characteristics reduce the total harmonic distortion but increase the filter size and inverter cost [4]. To overcome those problems, symmetrical MLIs have been proposed. Its structure is simple and reliable. It consists of auxiliary cell and one H-bridge cell. For increasing the level of inverter, additional auxiliary cells are connected in series. The special features of the symmetric MLI are low switching loss, low cost, low distortion, and the requirement of minimum switching devices [5]. In [6], the authors have presented a MLI which involves four basic structures to generate 15-level output. Each structure has six switches and two voltage sources. Therefore, the requirement of the number of switches and voltage sources is twenty-one and seven respectively. H-bridge and any additional circuit has not been used in this circuit for generating a negative level. The switching losses and conduction losses are less than conventional topology as lesser number of switches have been used. 15-level inverter has been designed in [7] with the number of IGBTs and voltages are sixteen and seven respectively. This topology also uses a smaller number of switches than conventional CHB MLI and the proposed in [6]. Subsequently, switching losses, conduction losses are also slighter than previously mentioned topologies. In [8], a new 15 level inverter has been suggested that utilizes ten switches, ten diodes and seven voltage sources. It offers better performance in terms of complexity, number of switches, distortion reduction, and size of the inverter circuit than that of the ones proposed [6]-[8]. In this paper, a new symmetric MLI has been proposed for grid-connected photovoltaic (PV) power plants. The proposed topology uses ten switches, six power diodes, and seven voltage sources for generating 15 level output. These reduced switching devices and power diodes make the inverter smaller in size, and light in weight. It also reduces losses and increases efficiency. A comparison has been done among the existing topologies and proposed topologies based on switching devices and power diodes count, cost, weight and total harmonic distortion (THD). For generating switching pulses, a new multicarrier topology named as a trapezoidal triangular

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carrier-based alternative phase opposition disposition (APOD) pulse width modulation (PWM) technique is proposed.

This paper has been organized as follows: section two deals with a brief description of the proposed inverter topology, section three deals with trapezoidal carrier based APOD PWM, section four deals loss calculation, section five deals with simulation results and performance analysis, section six deals with comparative study, and finally the article ends with conclusion and references.

II. PROPOSED SYMMETRIC MULTILEVEL INVERTER

Fig. 1 shows the proposed high frequency magnetic link (HFML)-based grid connected 15-level inverter topology. Here, for the maximum power point tracking (MPPT) operation, boost converter is considered. The medium frequency inverter is used to convert the array dc power to the medium frequency ac power.This Inverter also ensures the constant output voltage . The output of inverter is connected to the primary of HFML. The secondary of HFML is considered as an isolated source and connected to an H-bridge cell through a bridge rectifier. This HFML provides electrical isolation between PV array and grid, and also reduces common mode and voltage imbalance problems. This MPPT and magnetic link concept has been proposed in [9-10]. The different operating modes of the proposed inverter are shown in the Fig. 2.

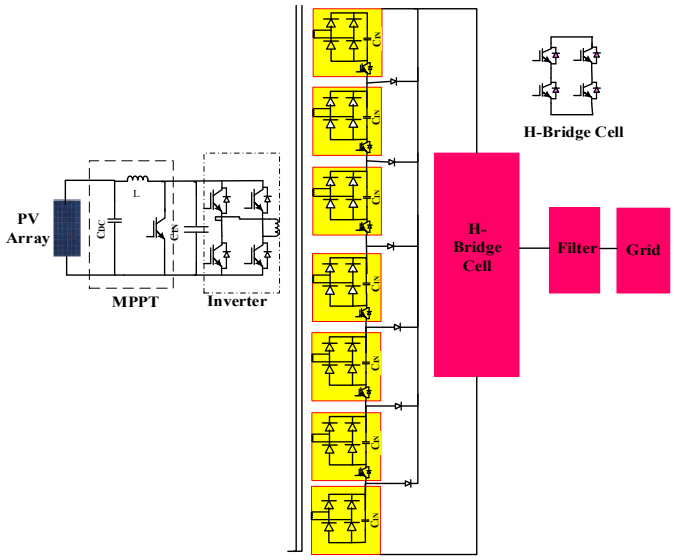

Fig. 1. Detailed circuit diagram of high frequency magnetic linked 15-level symmetric grid connected inverter.

A. Operation of the proposed Topology

In this sub-section, the operation of the proposed topology is discussed. This operation is divided into 15 modes which are discussed herein. During 'mode-1', the switches S_2 and S_4 are turned on and the current flowing through D_6, S_2 and S_4 as shown in Fig. 2(a). In this mode, the obtained output voltage is V. In 'mode-2', the switches S_5, S_2 and S_4 are turned on for generating output voltage of $2V$. The current path of this mode is shown in Fig. 2(b). During 'mode-3', the switches S_2, S_5, S_6, and S_4 are turned on and the current flows through D_4, S_2, S_5, S_6, and S_4 as shown in Fig. 3(a). In this mode, the obtained output voltage is $3V$. The 'mode-4' operation is appeared in Fig. 3(b). In this mode, the switches S_5, S_6, S_7, S_2, and S_4 are turned on for generating output voltage of $4V$. For generating output voltage of $5V$, the 'mode-5' is used. In this mode the switches S_5, S_6, S_7, S_8, S_2 and S_4 are turned on. This operation is shown in the Fig. 3(c). In 'mode-6', the switches S_5, S_6, S_7, S_8, S_9, S_2 and S_4 are turned on for generating output voltage of $6V$. The current path of this mode is shown in Fig. 3(d). In 'mode-7', the switches S_5, S_6, S_7, S_8, S_9, S_{10}, S_2, and S_4 are turned on for generating output voltage $7V$. The current path of this mode is shown in fig. 3(e). The 'mode-1, -2, -3, -4, -5, -6, -7' are termed as positive mode during which the gained voltage is positive. The 'mode-8, -9, -10, -11, -12, -13, -14' are christened as negative mode during which, the gotten voltage is negative. The 'mode-8' is just opposite to 'mode-1'. In this mode, the switches S_1 and S_3 are turned on for generating output voltage of '$-V$'. The operation is shown in Fig. 3(f). In 'mode-9', the switches S_5, S_1, and S_3 are turned on for generating output voltage $-2V$. The current path of this mode is shown in Fig. 3(g). Through 'mode-10', the switches S_1, S_5, S_6, and S_3 are turned on and the current flowing through D_4, S_1, S_5, S_6, and S_3 as shown in Fig. 3(h). In this mode, the obtained output voltage is $-3V$. During 'mode-11', the obtained voltage is $-4V$ by turning on switches S_5, S_6, S_7, S_1, and S_3 as shown in fig. 3(i). For generating output voltage $-5V$, the 'mode-12' is used. In this mode the switches S_5, S_6, S_7, S_8, S_1 and S_3 are turned on. This operation is shown in the fig. 3(j). In 'mode-13', the switches S_5, S_6, S_7, S_8, S_9, S_1, and S_3 are turned on for generating output voltage $-6V$. The current path of this mode is shown in Fig. 3(k). In 'mode-14', the switches S_5, S_6, S_7, S_8, S_9, S_{10}, S_1, and S_3 are turned on for generating output voltage $-7V$. The current path of this mode is shown in fig. 3(l). The 'mode-0' is obtained by turning on switches S_2 and S_3. The operation of this mode is shown in fig. 3(m). The switching pattern of this system is exposed in TABLE I.

B. Conventional Triangular Carrier Signal

In this sub-section, the calculated formula for the number of diodes, switches, and voltage sources are given. The complete number of levels that can be created for this circuit is determined by using equation (1)

$$N = 2m + 1 \tag{1}$$

The required number of switches required for generating desired output is obtained by using equation (2).

$$S = m + 3 \tag{2}$$

The required diode for proposed topology is determined by using equation (3)

$$D = m - 1 \tag{3}$$

where, m is number of voltage sources. N, S, and D represent the number of voltage levels, the number of switching devices, and the number of power diodes respectively. For example, for 15-level inverter, the proposed system requires seven voltage sources, ten switching devices, and six power diodes.

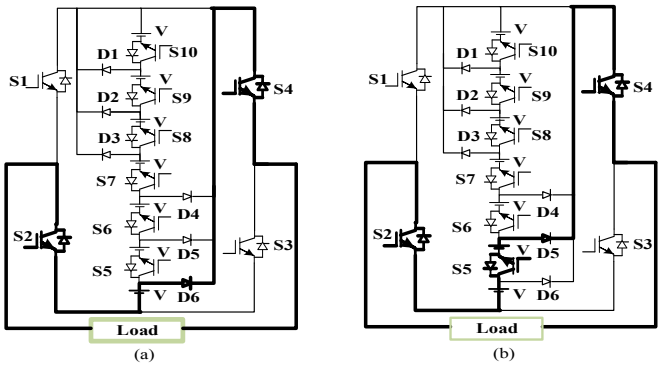

Fig. 2. The various voltage levels of the proposed topology (a) +V, (b) +2V,

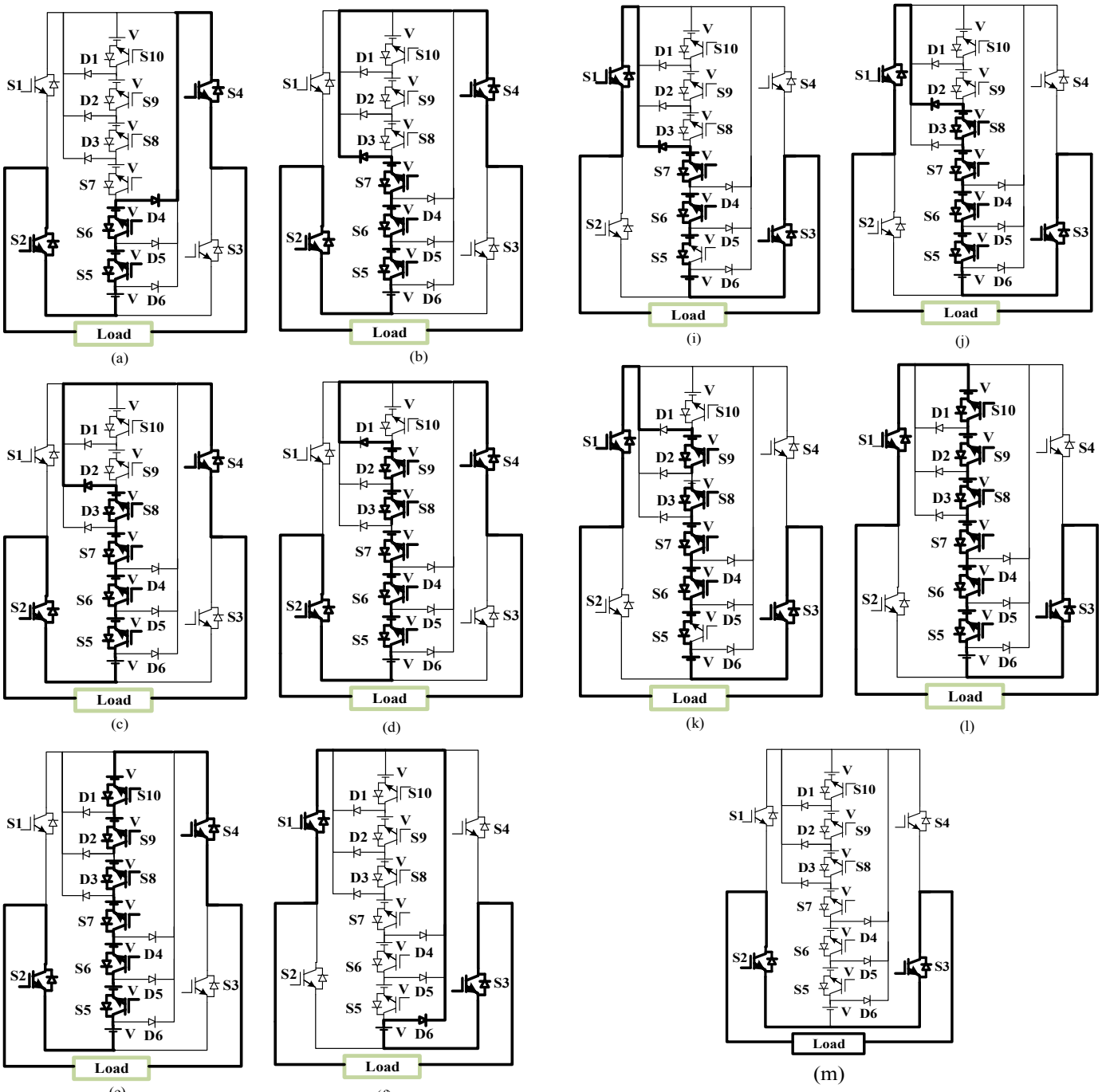

Fig. 3. The various voltage levels of the proposed topology (a) +3V, (b) +4V, (c) +5V, (d) +6V, (e) +7V, (f)-V, (g) -2V, (h) -3V, (i) -4V, (j) -5V, (k) -6V, (l) -7V, and (m) 0V.

III. Proposed Alternative Phase Opposition Disposition PWM

Level shifted PWM plays a vital role in generating switching pulses for cascaded and reduced switch inverters. In this topology, the carrier signal may be triangular, sawtooth signal, and trapezoidal signal. But the trapezoidal signal is better than the triangular signal which has been reported in [11]. Again in [14] it has been reported that the trapezoidal signal exhibits a better performance than other existing reference signals like sinusoidal signal, third harmonic injected signal, sixty-degree reference signal. For this purpose, trapezoidal carrier based phase opposition disposition (APOD) PWM is proposed in this paper. In this strategy, a few carrier signals are compared with a reference signal for generating switching pulses. For m level output, the requirement of carrier waves is (m-1). Every carrier signal has equal amplitude and

frequency. The frequency of the reference sign is 50Hz. Be that as it may, the frequency of a carrier signal might be multiple times in excess of a reference signal. Above the zero references, the output voltage will be positive when reference wave is greater than all upper carrier wave signals and bellow the zero reference, the output voltage will be negative when the reference wave is less than all lower carrier wave signals.

The magnitude difference between each carrier wave is calculated as

$$A_c = \frac{2A_m}{m-1} \tag{4}$$

where, m is the level of inverter, A_m is peak to peak magnitude of reference signal.

The modulation index can be calculated as

$$M_a = \frac{2A_m}{(m-1)A_c} \tag{5}$$

The frequency modulation index can be expressed as

$$M_f = \frac{f_c}{f_m} \tag{6}$$

where, f_c is the frequency of carrier signal and f_m is the frequency of message signal.

In trapezoidal triangular carrier based alternative phase opposition disposition trapezoidal PWM, all carrier signals are out of phase with each other. APOD scheme for proposed inverter is presented in Fig. 4.

TABLE I
SWITCHING PATTERN FOR PROPOSED SYMMETRIC 15-LEVEL INVERTER

VOLTAGE LEVELS	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
0	0	1	1	0	0	0	0	0	0	0
V	0	1	0	1	0	0	0	0	0	0
2V	0	1	0	1	1	0	0	0	0	0
3V	0	1	0	1	1	1	0	0	0	0
4V	0	1	0	1	1	1	1	0	0	0
5V	0	1	0	1	1	1	1	1	0	0
6V	0	1	0	1	1	1	1	1	1	0
7V	0	1	0	1	1	1	1	1	1	1
-V	1	0	1	0	0	0	0	0	0	0
-2V	1	0	1	0	1	0	0	0	0	0
-3V	1	0	1	0	1	1	0	0	0	0
-4V	1	0	1	0	1	1	1	0	0	0
-5V	1	0	1	0	1	1	1	1	0	0
-6V	1	0	1	0	1	1	1	1	1	0
-7V	1	0	1	0	1	1	1	1	1	1

Here for generating 15 level output, total 14 carrier waves are used. The magnitude of each carrier is 0.143 p.u. and the frequency of each carrier is 1kHz.

IV. LOSS CALCULATION

Mainly two types of loss termed as conduction loss and switching loss are calculated in this paper. Conduction loss occurs during the power devices is the on state and Conducting current. On the other hand, the switching loss occurs due to turn on or off of switch and diode.

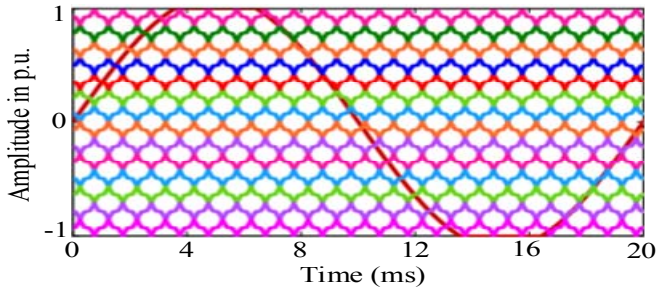

Fig. 4. Proposed carrier signal arrangement for 15-level inverter.

Here, IGBT FF150R12KT3G are considered for loss calculation. Mathematical models obtained for the IGBT module FF150R12KT3G [11] are given by

$$V_{ce} = 1.15e^{0.00226I(\theta)} - 0.6654e^{-0.044I(\theta)} \tag{7}$$

$$V_F = 1.2e^{0.002I(\theta)} - 0.72584e^{-0.0475I(\theta)} \tag{8}$$

$$E_{on} = 0.0051e^{0.0064I(\theta)} - 0.0037e^{-0.00811I(\theta)} \tag{9}$$

$$E_{off} = 0.0643e^{0.00121I(\theta)} - 0.0647e^{-0.00107I(\theta)} \tag{10}$$

$$E_{rec} = 0.01806e^{0.000412I(\theta)} - 0.0157e^{-0.06736I(\theta)} \tag{11}$$

$$I(\theta) = M * I_{max} Sin(\theta - \emptyset) \tag{12}$$

where, M is the modulation index, $\emptyset$ is the phase shifted between voltage and current, $V_{ce}(\theta)$ is the voltage across switch, and $V_F(\theta)$ is the voltage across diode, E_{on} is the turn on commutation, E_{off} is the turn off commutation, and E_{rec} is the diode reverse recovery process. This model is found using the points extracted of datasheets of each semiconductor and using MATLAB curve fitting tool.

The calculation of conduction power losses can be given by

$$P_{cond\_IGBT} = \frac{1}{2\pi}\int_0^{2\pi} V_{ce}(\theta) \times I(\theta) \times V_{cmd}(\theta)\, d\theta \tag{13}$$

$$P_{cond\_D} = \frac{1}{2\pi}\int_0^{2\pi} V_F(\theta) \times I(\theta) \times V_{cmd}(\theta)\, d\theta \tag{14}$$

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_D} \tag{15}$$

The switching loss can be calculated as

$$P_{sw} = \frac{1}{T}\sum E_{on} + E_{off} + E_{rec} \tag{16}$$

Here, only switching loss is considered for analysis.

V. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

In this section, the ability of the proposed inverter has been examined by MATLAB/ Simulink software package. Simulation is done for trapezoidal carrier based APOD PWM strategy as discussed previously and for different values of M_a ranging from 0.8 – 1.2 and M_f ranging from 20 – 100. During the simulation, each dc voltage is fixed as 50V, Load resistance is selected as 100Ω and load inductance is 50mH and the carrier frequency is fixed as 1kHz. Fig. 5 and Fig. 6 show the output voltage and harmonics spectrum of the proposed topology with filter and without filter respectively.

The performance of proposed APOD PWM technique is also analyzed in this section. This analyzation is done by varying amplitude modulation index and frequency modulation index. The aim of this section is to find optimum condition for which the minimum THD and maximum fundamental output voltage are obtained.

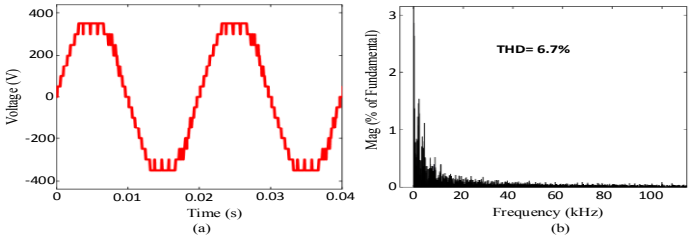

Fig. 5. Output voltage and harmonic spectrum of proposed MLI without filter.

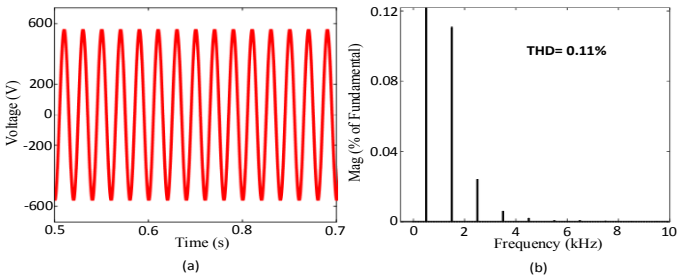

Fig. 6. Output voltage and harmonic spectrum of proposed MLI with filter.

A. Amplitude Modulation Index Variation

The performance of proposed symmetric 15-level inverter depends on amplitude modulation index variation. So, modulation index is an important factor. Measuring the THD for proposed inverter at a modulation index from 0.8 to 1.2, it is seen that THD varies randomly for the variation of a modulation index. THD is measured in percentage here. When modulation index variation is done, the frequency of carrier signal is fixed at 1 kHz.

From the TABLE II, it is seen that THD decreases with increasing modulation index during under modulation index but in overmodulation region, THD increases with increasing modulation index. The optimal THD is obtained during normal modulation index. Note that, fundamental output voltage rises in overmodulation region.

B. Frequency Modulation Index Variation

The performance of proposed symmetric 15-level inverter depends on frequency modulation index variation. So, frequency modulation index is also an important factor. Measuring the THD for proposed inverter at frequency modulation index from 20 to 100. The obtained result is shown in the TABLE III.

From the TABLE III, it is seen that the THD variation for proposed symmetric 15- level inverter for the proposed PWM scheme is too fluctuating. It shows the lowest THD at frequency modulation index 20.

TABLE II
CALCULATED THD FOR AMPLITUDE MODULATION INDEX VARIATION

Amplitude Modulation Index	THD (%)	Fundamental Output Voltage(V)
0.8	9.6	214.7
0.9	8.6	235.7
1	6.7	264.0
1.1	9.47	276.3
1.2	12.11	284.0

TABLE III
CALCULATED THD FOR FREQUENCY MODULATION INDEX VARIATION

Frequency Modulation Index	THD (%)	Fundamental Output Voltage(V)
20	6.7	264
40	7.41	265
60	7.23	265.2
80	7.13	264.9
100	7.39	264.5

C. Calculated Loss for Modulation index Variation

In this subsection, the switching loss is tabulated for modulation index 0.8 to 1.2 in TABLE IV.

TABLE IV
SWITCHING LOSS VARIATIONS WITH DIFFERENT MODULATION INDICES

Modulation Index	Switching Loss (W)
0.8	0.874
0.9	1.11
1	1.14
1.10	1.169
1.20	1.31

From TABLE IV, it is understood that the switching loss is increased as the modulation index increases.

VI. COMPARATIVE STUDY

In this section, the comparison among proposed and existing symmetric 15-level inverter has been done with the help of simulation results. The comparison has carried out based on the number of switching devices and power diodes, cost, weight, and THD values.

TABLE V
COMPARISON OF DIFFERENT MULTILEVEL INVERTER TOPOLOGIES

Inverter	No. of Levels (N)	No. of Switches (N_s)	No. of diodes (N_d)	Ratio (N_s/N)	Ratio (N_d/N)
DC	15	28	182	1.87	12.13
CHB		28	-	1.87	0
FC		28	-	1.87	0
NPC		28	26	1.87	1.73
Ref. 6		21	-	1.4	0
Ref. 7		16	-	1.07	0
Ref. 8		10	10	0.67	0.67
Proposed		10	6	0.67	0.40

From the TABLE V, it is clear that among the conventional topologies, the DC topology requires 1.87 switching devices and 12.13 power diodes, and, the CHB and FC topologies use 1.87 switching devices but they don't use power diodes, and also, the NPC topology utilizes 1.87 switching devices and 1.73 power diodes for generating one level of output voltage. Because of the large number of switches, the switching losses and conduction losses are more in conventional topologies. Due to increased losses in conventional topologies, the efficiency decreases. Some recently published symmetrical 15-level inverter topologies are also shown in this TABLE V. It is seen that, among those recent published topologies, the proposed and [8] use only 0.67 switching devices for generating one level output voltage. But the proposed topology uses only 0.40 power diodes which is lesser than [8]. Because of low switching devices, the switching losses and conduction losses will be lower than

conventional and mentioned reference topologies which ensure the better performance of the proposed topology.

A. Comparison based on Cost & Weight

Cost comparison is done for each inverter by calculating the cost of switch, power diodes, and capacitors of the inverters. The switches, capacitors, and diodes are considered for all of the inverters to have a more accurate comparison. The IGBT FF150R12KT3G, diodes 85HF60, and capacitor C4DEFPQ6380A8Tk are used for comparison [15]. The weight and cost comparison for all types of symmetric inverter are shown in TABLE VI.

From the above table, it is seen that the cost and weight of proposed inverter are less than existing conventional and recently published symmetric inverters. Therefore, the size of the proposed inverter becomes slighter and the weight becomes lighter. So, it is more efficient than other existing topologies.

TABLE VI
COST AND WEIGHT COMPARISON OF DIFFERENT MULTILEVEL INVERTER TOPOLOGIES

Inverter	Weight (K. g.)	Price (US€)
DC	18.48	5494.272
CHB	9.52	2913.96
FC	85.778	23279.396
NPC	15.828	4625.352
Ref. 6	7.14	2185.47
Ref. 7	5.44	1665.12
Ref. 8	3.57	1096.4
Proposed	3.50	1074.12

B. Comparison based on Total Harmonic Distortion(THD)

In this subsection, the comparison among proposed and existing topologies has been carried out depending on total harmonic distortion. Here, the proposed model is compared with cascaded H-bridge, diode clamp and recently publish few papers. The result of the comparison has been shown in the following figure. From this figure it is seen that our proposed topology offers low THD than other topologies.

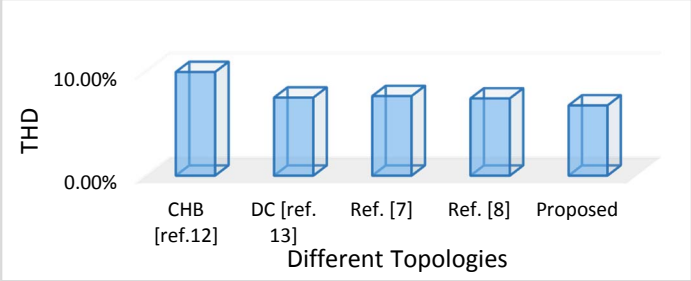

Fig. 7. THD comparison among different topologies.

VII. CONCLUSIONS

In this paper, a new symmetric 15-level inverter is proposed, which utilizes ten semiconductor switches, six control diodes, and seven voltage sources for creating 15-level output voltage. From the above discussion, we find some important features of the proposed MLI topology, like (i) lower number of components, (ii) smaller size and light weight, (iii) less THD, (iv) low cost, and (IV) decreased switching loss as well as increased overall efficiency. Using the idea of this topology, a sustainable and energy efficient solar power system can be implemented in future with lower complexity.

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